Master Course Syllabus for EE 271 (ABET sheet)

Title: Digital Circuits and Systems

Credits: 5 (4 lecture, 1 lab)

UW Course Catalog Description

Overview of digital computer systems. Covers logic, Boolean algebra, combinational and sequential circuits and logic design; programmable logic devices; and the design and operation of digital computers, including ALU, memory, and I/O. Weekly laboratories. Cannot be taken for credit if credit received for CSE 369. Prerequisite: either CSE 121, CSE 122, CSE 123, CSE 142, or CSE 143.

Coordinator: S. Hauck, Professor, Electrical and Computer Engineering

(Team) Faculty who have or are willing to teach this core course):
Mahmood Hameed, Scott Hauck, Rania Hussein, Sep Makhsous, Denise Wilson

Goals: To provide a fundamental understanding of digital hardware systems and their design.

Note: EE-271 is tightly coupled with CSE-369, with the expectation that students that complete either EE-271 or CSE-369 will have reached a similar level of understanding of the design of digital circuits and systems.

Learning Objectives: At the end of this course, students will be able to:

1. *Design* and *implement* simple combinational circuits using basic logic gate chips.
2. *Write* Boolean equations to describe basic combinational logic circuits
3. *Use* Boolean algebra to simplify such equations, then implement the resulting designs in the laboratory.
4. *Design* and *implement* combinational circuits of medium complexity in the laboratory.
5. *Design* and *implement* basic sequential circuits and finite state machines in the laboratory.
6. *Identify* real world timing problems in both combinational and sequential circuits and design basic digital systems that resolve or mitigate such problems.
7. *Design* and *implement* combinational and sequential circuits using programmable logic devices.
8. *Develop* basic structural models of digital systems using the Verilog hardware design language.

Textbook (recommended):
Harris & Harris, *Digital Design and Computer Architecture: ARM Edition, 1st* Ed., Morgan Kaufmann, 2015.

Prerequisites by Topic:
1. Familiarity with basic software programming and debugging techniques.

Lecture Topics:

1. Number systems: positional number system, negative number representation.

2. Boolean algebra: logic gates, basic theorems of Boolean algebra, minimization by formulas, incompletely specified functions.

3. Combinational circuit design; integrated circuit characteristics, encoders, decoders, multiplexers, arithmetic operations.

4. Sequential logic design using DFFs. Designs include shift registers, counters, and sequential circuits (including state diagrams and state tables, and the resulting circuit implementations).

5. Programmable logic devices: Field Programmable Gate Arrays (FPGA) and applications of programmable logic devices.

Laboratory Topics:
There are weekly laboratory assignments, and a final project. All offerings of this course use the same standardized labs, lab kit, and lab equipment. These are maintained by the course coordinator, with oversight from the core curriculum committee. For summer offerings, due to the compressed timeline, some consecutive labs may be combined together.

- *Lab 1:* basic TTL circuits on the breadboard.
- *Lab 2*: multi-level logic on the breadboard. Basic gate-level SystemVerilog and FPGA designs.
- *Lab 3:* more complex multi-level logic in SystemVerilog and FPGA designs. Don't cares.
- *Lab 4*: RTL circuits in System Verilog.
- *Lab 5:* basic sequential logic.
- *Lab 6*: systems of multiple sequential logic circuits interacting together to achieve an overall design.
- *Lab 7*: Counters, LFSRs, comparators, and other arithmetic circuits.
- *Lab 8 (multiple weeks)*: final project. A complex System Verilog design and FPGA hardware implementation, similar in complexity to a hand-held game, complex traffic light system, or the equivalent. Brings together all elements of the class into a multi-week final project.

Course Structure: The main lecture meets for four 50-minute session per week, or two 110-minute sessions per week.

The organization and delivery style of EE271 lectures is at the discretion of the instructor. Lecture sessions typically consist of lecture interspersed with (a) examples which illustrate the application of important concepts; (b) demonstrations which illustrate these principles at work in real devices; or (c) student-centered activities including small group problem solving activities and think/pair/share exercises designed to reinforce understanding of basic concepts and resolve misconceptions.

Computer Resources: There will be extensive computer usage in the laboratories for design and simulation with the SystemVerilog hardware description language and FPGA software packages.

Laboratory Resources: Students are loaned a laboratory kit including an FPGA board, some simple TTL chips, and supporting elements. For each laboratory, the students have to design the circuit, construct it and demonstrate it to the instructor and/or teaching assistant using this physical kit. The final project may be via physical kits, remote hub, or another modality as determined by the course instructor.

Grading: Assignments in the course consist of weekly homeworks, lab assignments (including a final project), exams, and (depending on instructor) in-class exercises of quizzes. Specific point distributions are at the discretion of the instructor.

Labs can be done solo, or in pairs, at the discretion of the instructor. For pairs, it is highly recommended that part of the lab assignment grading include a direct, face-to-face laboratory demonstration that verifies that each student is learning the hands-on laboratory skills for which the course is designed and also minimize academic dishonesty. If students work in teams to complete the laboratories, a means for ensuring that each student contributes something meaningful to each laboratory solution is strongly recommended. Homeworks may be completed in teams or solo (at the discretion of the instructor) while summative assignments (exams, quizzes) etc. should be completed solo.

ABET Student Outcome Coverage: This course addresses the following outcomes:
H = high relevance, M = medium relevance, L = low relevance to course.

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(1) *An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics* **(H)**

(2) *An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors* **(M)**

(3) *An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions* **(L)**

(4) *An ability to acquire and apply new knowledge as needed, using appropriate learning strategies* **(L)**

Prepared By: Scott Hauck
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Additional information and resources regarding teaching ECE courses (e.g., links to course repositories for materials from previous course offerings; guidelines for using AI tools in courses; syllabus language for course accommodations, etc.) can be found on the UW ECE Intranet:
https://peden.ece.uw.edu/academic-ops/