

Master Course Description for EE-371 / CSE-371 (ABET sheet)

Title: Design of Digital Circuits and Systems

Credits: 5 (4 lecture; 1 lab)

UW Course Catalog Description

Coordinator: Rania Hussein, Associate Teaching Professor, Electrical and Computer Engineering

Goals: The execution of modern digital electronic systems designs presents challenges that demand new ways of thinking about such problems. Building upon the fundamental concepts of electronic circuits and those developed in EE 271, the main objective of EE 371 is to provide students with a theoretical background to and practical experience with the tools, techniques, and methods for solving challenges related to modeling complex systems using the Verilog hardware description language (HDL), signal integrity, managing power consumption in digital systems, and ensuring robust intra and inter system communication.

We will work with the Altera DE1-SOC development board that utilizes the Cyclone V FPGA combined with a variety of peripheral devices, including the embedded NIOS II processor, as our target hardware platform. The hardware side of the applications will be specified then designed, modeled, and tested using the Verilog HDL and the libraries and tools provided under the Quartus II development environment. We will synthesize then download the tested modules onto the DE1-SOC board where they will be integrated into a complete working system. The software side of the applications will be written in C, cross-compiled under the NIOS II IDE then downloaded and executed on the embedded NIOS II processor.

Upon completion of the class the student will have developed strong design skills for implementing complex digital logic systems in modern design languages onto FPGAs and similar programmable fabrics.

Learning Objectives: At the end of the course, students will be able to:

1. *Identify and understand* real-world timing problems in both combinational and sequential circuits,
2. *Understand and recognize* the parasitic elements of circuit traces, the interactions between traces, and the affects of such interactions as well as affects from the outside world on circuit signal integrity.
3. *Understand and design* intra and inter system communication and timing in systems comprising components operating with differing (asynchronous) timing, multiple clocks, and clocking schemes.
4. *Design, model, and implement* intermediate level digital systems that are tolerant of real-world timing effects.

5. *Design and implement* schemes to measure, manage, and reduce power consumption in digital designs.
6. *Understand and design* systems comprising networks of distributed components or subsystems.
7. *Design and Implement* a system supporting a contemporary network interface standard.

Textbook: John F. Wakerly, *Digital Design Principles and Practices*, Prentice-Hall, 4th Ed., 2006.

Supplemental and Reference Materials:

1. Documents related to Verilog, Gate Array and Complex Programmable Logic Devices, Signal Integrity, and Power Management.
2. Altera pcbLayoutstx2_sii52012.pdf
3. PCBLayoutEst-wced06.pdf
4. Michael D. Ciletti, *Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL*, Prentice Hall, 1999.
5. Howard W. Johnson and Martin Graham, *High Speed Digital Design - A Handbook of Black Magic*, Prentice Hall, 1993.
6. Douglas Brooks, *Signal Integrity Issues and Printed Circuit Board Design*, Prentice Hall PTR, 2003.
7. Geoff Lawday, David Ireland, and Greg Edlund, *A Signal Integrity Engineer's Companion*, Prentice Hall, 2008.
8. Andrew Tanenbaum, *Computer Networks*, Prentice Hall, 2003.

Prerequisites:

1. either EE-205 or EE-215
2. either EE-271 or CSE-369

Topics:

1. Verilog HDL and HDL Modeling at the Dataflow and Behavioral levels, 2.0 weeks
2. Datapath and Control Components in a digital system, 1.0 week
3. Timing and Practical Considerations, 1.0 week
4. Introduction signal integrity and signal integrity issues, 2.0 weeks
5. Power management in digital systems, 1.0 week
6. Introduction to networks and basic network concepts, 2.0 weeks
7. Testing and design for test in digital systems, 1.0 week

Course Structure: The course meets for 4 hours of lecture and 3 hours of laboratory.

Computer Resources: There will be extensive computer usage in the homework and laboratories for design and simulation utilizing the Verilog HDL and FPGA device software development packages.

Laboratory: There are weekly laboratory projects. For each such project, the students have to design the circuit, construct it and demonstrate it to the instructor and/or teaching assistant. In all of the projects, the students use programmable logic devices and microprocessors for implementation with the designs developed using the Verilog HDL. All laboratories are done in an open lab as two or three person teams.

Grading: The grade is based upon weekly homework assignments, the laboratory projects, midterm exams, and a comprehensive final examination.

ABET Student Outcome Coverage: This course addresses the following outcomes:

H = high relevance, M = medium relevance, L = low relevance to course.

- (1) *An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics. (H)* These are all done as an integral and routine part of the material taught. Theory is presented a standard part of the homeworks, exams, and laboratories in the context of its application to real-world problems and its limitations under real-world constraints.
- (2) *An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. (H)* Each of the laboratory projects specifies and assigns a particular design problem to be solved.
- (3) *An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions. (H)* Students will use modern computers, test instrumentation, modeling, and simulation tools. A significant component of designing and developing a real-world application is ensuring that one's system performs to specification in the intended environment. Such assurance can only be gained by testing the system in such a context then analyzing the results of those tests. Such a process is integral to this class, to each of the labs and to the final project.

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