EE478/EE526 Syllabus

Title: Capstone Integrated Digital Design Projects
Credits: 5

UW Course Catalog Description

Coordinator: Visvesh S. Sathe
Course Goals:

1. Capstone VLSI design involving a major design experience in completing the physical design of a substantial digital system (e.g. a RISC processor) with enhancements that are either in circuit construction (dynamic logic, custom datapaths), architectural (microarchitectural enhancements such as out-of-order execution) or methodology driven (power-gating, clock gating, sub-threshold or near-threshold design).
2. Understand and apply best-practices toward building digital systems in the areas of analysis, construction, and verification. Support these design efforts through instruction of technical concepts in high-speed design, timing optimization, power management, clocking and timing analysis.
3. Use industry standard design tools to design VLSI structures for custom and automated physical design, simulation and verification that complement lecture material.
4. Project: student will work in teams to design a VLSI system targeted toward a real-world application. Team-based projects encourage effective team and project management in the context of a rigorous technical design experience.

Learning Objectives:

1. A strong grasp of the fundamentals of VLSI circuits and systems, with a particular emphasis in making connections between low-level theoretical concepts (power, delay, wire-parasitics, noise-margins), architecture-level considerations (latency of data-movement, the case for heterogeneous computing), and a student-group defined application. Once these connections are made, the student-teams need to plan on executing a design that fulfills the stated objectives.
2. A strong grasp of planning, analysis, preparation, and execution of high-quality system designs.
3. Developing the fundamentals for design for test, and standard verification techniques in design.

Textbook: Weste & Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Addison-Wesley, 2010

Prerequisites by Topic:

1. Introduction to VLSI design (EE476)
2. Knowledge of ASIC design flows is strongly recommended (EE477)

Course Structure: There are 4 hours of lecture per week, plus 1 hour of discussion. The discussion will be used for student presentations of project progress, and tips-and-tricks for tool-flows needed to implement the digital IC projects. The course will contain very little by way of new learning. Instead, the focus will be on enabling students to define, plan and execute their capstone project effectively. The project is grounded in the context of a baseline microprocessor around which student-groups need to build an application-specific system. Doing so involves designing upgrades or "add-ons" to the processor architecture, additional modules and/or accelerators, or design methodologies to achieve a desired application objective (e.g. sub-threshold computing for ultra-low power sensor nodes). A robust lab component is offered initially to provide students with the tools and infrastructure they need to

execute on the project. A significant portion of the learning in this course happens in the student design labs through peer interaction, and that with the TA who holds regular office hours in the design lab.

Grading:

- Assignments (20%)
- Project (70%)
- Final Exam (10%)

Distinguishing Graduate and Undergraduate Components: Graduate students are expected to perform two additional add-ons or upgrades compared to undergraduates. While undergraduates are expected to design only a single upgrade or add-on, graduate students will be expected to deliver three of these add-ons. Expectations on the level of verification to be demonstrated for these add-ons remains consistent across undergraduate and graduate students.

Syllabus: Note. Items Marked (T) are theory learning topics that remain in the course

Week No.	Lecture Topics	Discussion Topics	HW/Peer assessment /Project write-ups
1	Introduction, CMOS Scaling	Project planning	
2	Practical Gate Design w/ Logical Effort	Using Makefiles	Project Proposals due
3	Course proposal presentations, Clocking(T)	Intro to design toolflow (1)	
4	Wires, Dynamic Logic (T)	Intro to design toolflow (1)	
5	Design for Test considerations for your design	Intro. To python for VLSI	Design review slides ready
6	Mid-term Design Review	Feedback on Design review presentation and delivery	
7	Practical low-power techniques and application	Design Verification techniques	
8	DLL and PLL design (T)	Project delivery spec.	
9	Slack slots (to cover variation of above topics in the class based on project mix)		Final course presentation slides due
10	Final Course Presentations		Peer Evaluation Due

Religious Accommodations

Washington state law requires that UW develop a policy for accommodation of student absences or significant hardship due to reasons of faith or conscience, or for organized religious activities. The UW's policy, including more information about how to request an accommodation, is available at Religious Accommodations Policy (https://registrar.washington.edu/staffandfaculty/religious-accommodations-policy/). Accommodations must be requested within the first two weeks of this course using the Religious Accommodations Request form (https://registrar.washington.edu/students/religious-accommodations-request/).

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