**Master Course Description for EE 435/EE 5XX (ABET sheet)**

**Title:** Linear Integrated Circuits

**Credits:** 5

**Offered:** Fall Quarter

**UW Course Catalog Description:** The course will focus on the design of analog integrated circuits that are classified as linear. Common examples include linear amplification of signals, generation of DC sources, and accurate replication of DC bias circuits. The course material includes a review of simple single-transistor amplifiers, followed by the design of low-noise, temperature-voltage-process independent bias circuitry, transistor-level design of operational amplifiers, impact of device mismatch on circuit performance, stability and compensation of feedback circuits.

**Coordinator:** Chris Rudell, Professor, Electrical and Computer Engineering

**Course Description:** Introduction to Linear Integrated Circuit Design. Topics include integrated circuit analysis and design, small- and large-signal device and circuit modeling, amplifier design, bias circuit design, frequency response, stability and the use of circuit frequency compensation techniques to improve stability. Knowledge gained from this course can be applied to a broad set of integrated circuit applications including chips for wearable and implantable biomedical electronics, communications systems, radar, high-speed data transfer, analog neural networks and "in-memory compute", to name a few.

**Prerequisites:** EE 332, EE 333 or equivalent from another institution.

**Recommended courses:** EE 331, EE 361.

**Coordinator:** Chris Rudell, Professor, Electrical and Computer Engineering

**Learning Objectives:** At the end of this course, students will be able to:

1. *Analyze* analog linear integrated circuits from basic single-transistor amplifiers to differential pairs, to complex multi-stage operational amplifiers.
2. *Develop Skills* using linear small-signal analysis concepts to determine the gain, bandwidth and equivalent input/output resistance/impedance of circuits. Fundamental concepts in feedback and stability, with an introduction to frequency compensation techniques to ensure stability over a wide range of operating conditions are explored.
3. *Develop an Understanding* of performance parameters in modern semiconductor technologies that include Process, Temperature and Voltage (PVT) variation, and device mismatch.
4. *Develop* Skills that all analysis of differential circuits using the half-circuit method.
5. *Design* of PVT independent DC bias voltage/currect sources, current mirrors, and Bandgap voltage sources.
6. *Design* circuits which are cost effective (minimum silicon footprint), appropriate for advanced semiconductor manufacturing with high yield (99%+),
7. *Develop Proficient Knowledge* of real-world CAD Tools coupled with modern process and design kits (PDKs).

8. *Design* of CMOS operational amplifiers with an emphasis on amplifiers placed in closed-loop feedback and designing proper compensation for feedback loops.

**Additional Learning Objectives for EE 5xx:** At the end of this course, graduate students will be able to:

1. *Analyize:* circuit design projects from a system perspective. Graduate students will need to analyze the quantitative impact of their circuit design projects on the system level performance. This can be done through modeling using Verilog-A or Matlab, to evaluate commonly accepted system-level figures of merit (FoM).
2. *Model:* the entire chip architecture using Verilog-A or the equivalent system model tools.
3. *Lead* small circuit design teams which include undergraduate students who will benefit learning from more senior students.

**Course materials:** Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd Ed., New York: McGraw-Hill, 2017.

**Prerequisites:**

1. Analog Devices and Circuits (EE 332), Analog Embedded Systems (EE 333).
2. Understanding of basic electromagnetic principles is recommended (EE 361).
3. Working knowledge of diodes and basic logic circuits is recommended (EE 331).
4. Deep knowledge of single-transistor MOSFET amplifier configurations such as common-source (CS), common-gate (CG), and common-drain (CD) amplifiers. This includes understanding the role of each amplifier in building larger analog circuits. Moreover, understanding how to derive the input/output impedance, small-signal gain and bandwidth of CS, CG and CD amplifiers is assumed at the beginning of EE 435.
5. Requires the necessary analytical skills to find the gain, impedance and bandwidth of differential circuits including the half-circuit analysis method.
6. Knowledge of simple DC bias circuits including current mirroring techniques, design of current and voltage sources.
7. Basic understanding of closed-loop feedback using amplifiers.
8. Comfortable with the frequency-response analysis and simulation of circuits in the frequency domain.
9. Working knowledge of Linux and Cadence to simulate circuits in the time and frequency domain.

Syllabus:

1. Introduction and Applications using Linear Analog ICs (chips) – 1.0 week
2. Review and in-depth look at device modeling and physics– 1.0 week
3. Transistor-level frequency response- 1.0 week
4. Circuit noise and analysis – 1.0 week
5. Bias circuit design issues (current and voltage – e.g. bandgap) – 2 weeks
6. Operational amplifier (topologies) - 1 week
7. Feedback, stability and frequency compensation - 2 weeks
8. Design Project Presentations and advanced topics – 0.5 week

**Course Structure:** The class nominally meets for four 50-minute lectures per week. An additional 50-minute session led by either the TA or professor can be used as a discussion session to present example problems, or a regularly lecture. There are approximately six to seven homework assignments that include small SPICE simulation projects. There are multiple design projects that require Spectre (RF) simulation for verification of specifications; the projects include written presentations. There are nominally four small quizzes throughout the quarter with a midterm and in some quarters a final exam; some quarters there is a larger final project and the final exam is omitted.

**Computer and Laboratory Resources:** The computer simulations (HSPICE, PSPICE, or SPECTRE) can be done on any laptop with VNC installed (or equivalent virtual desktop) and logging into the instructional machines found 3rd floor of the Electrical and Computer Engineering building lab, currently serving as the ECE Department educational machines.

**Grading:**

- Homework (15%): Grad students will be given more complex homework sets.
- Two Design Projects (40%): Design projects defined by the lecturer. Students will be expected to design, layout and verify the circuit-based projects. Graduate students will have additional which will include circuit design, layout and verification. Graduate students will be given more advanced projects that relate circuit blocks to system-level performance.
- Four quizzes (20%): Quizzes will cover material related to the homework assignments.
- Midterm (10%): Midterm will be given toward the end of the quarter.
- CAD tutorials (15%): Tutorials on Cadence-based simulation for analog circuits and systems.
- No final examination.

**ABET Student Outcome Coverage:** This course addresses the following outcomes:

H = high relevance, M = medium relevance, L = low relevance to course.

(1) *An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics*. (**H**) The vast majority of the lectures, homework and projects deal with the application of circuit theory and control theory to specific linear integrated circuit operation. Large- and small-signal semiconductor device characteristics are included in the formulations. Linear circuit analysis formulations are commonplace throughout the course. The homework and examinations involve solving engineering problems identified by the assignments and exemplified by class discussion. The design projects challenge the students to identify the issues and formulate their individual solutions. The projects are conducted in teams of two. Since both MOS and BJT technologies offer two major device options, each team member chooses one of the two options. The team submits a written report describing the individual designs and comparing the two alternative implementations.

(2) *An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and*

*economic factors*. (**L**) The course covers analysis and with emphasis on synthesis of linear integrated circuits, with associated homework and examination problems. To incorporate realistic constraints, a module on integrated circuit process variations and yield is taught.

(3) *An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions*. (**L**) Students use SPICE to simulate homework problems and to support the design projects.

**Religious Accommodations:**

> "Washington state law requires that UW develop a policy for accommodation of student absences or significant hardship due to reasons of faith or conscience, or for organized religious activities. The UW's policy, including more information about how to request an accommodation, is available at Religious Accommodations Policy (https://registrar.washington.edu/staffandfaculty/religious-accommodations-policy/). Accommodations must be requested within the first two weeks of this course using the Religious Accommodations Request form (https://registrar.washington.edu/students/religious-accommodations-request/)."

**Accommodations & Access:**

> "If you have already established accommodations with Disability Resources for Students (DRS), please communicate your approved accommodations to the instructor at your earliest convenience so we can discuss your needs in this course. If you have not yet established services through DRS, but have a temporary health condition or permanent disability that requires accommodations (conditions include but not limited to; mental health, attention-related, learning, vision, hearing, physical or health impacts), you are welcome to contact DRS at 206-543-8924 or uwdrs@uw.edu or disability.uw.edu. DRS offers resources and coordinates reasonable accommodations for students with disabilities and/or temporary health conditions. Reasonable accommodations are established through an interactive process between the student, instructor, and DRS. It is the policy and practice of the University of Washington to create inclusive and accessible learning environments consistent with federal and state law."

**Prepared By:** Chris Rudell

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