Master Course Description for EE-436/EE 5XX, EE-437/EE 5XX (ABET sheet)

Title: Integrated Systems Capstone I, II

Credits: 5, 5

Offered: Winter, Spring (2 quarter sequence)

UW Course Catalog Description: This is a two-course sequence that culminates in a chip tapeout and fabrication, building on concepts from EE 435 to realize analog and mixed-signal systems-on-a-chip. Students working in teams start the design process of an analog/mixed-signal/RF System-on-a-chip in EE 436, and then continue with chip layout, verification and final tapeout in EE 437.

Prerequisite: EE 435 is required for EE 436, and EE 436 is required for EE 437.

Prerequisites by Topic:

1. Analog simulator proficiency (SPICE, Spectre, SpectreRF, covered in EE 332)
2. Schematic capture proficiency (Cadence design tools)
3. Electronic device large and small-signal modeling (MOSFET; covered in EE 332)

Students should be comfortable with the design of linear operational amplifiers, design of bandgap reference voltages, current sources, low-voltage current-mirroring techniques, and have strong fundamentals with respect to frequency response analysis, as well as the application of Kirchoff's current and voltage law.

Recommended: EE 331 and EE 361.

Coordinator: Chris Rudell, Professor, Electrical and Computer Engineering

Goals: This course sequence provides students with practical and theoretical foundations in integrated circuit and system design using contemporary CAD tools and modern semiconductor technologies. Through a two-quarter, project-based experience, students will design and implement a complete system-on-chip (SoC) tailored to an application area of their choice, such as communication systems, biomedical systems, control, or power electronics. Their designs may incorporate digital, analog, mixed-signal, and RF components. By the end of the sequence, each student team will have produced a fully verified chip design ready for fabrication, pending available funding. The course emphasizes hands-on learning, professional circuit design methodology, and the end-to-end workflow used in today's semiconductor industry.

Learning Objectives:

At the end of this course, students will be able to:

1. *Calculate* the frequency compensation necessary to stabilize any circuit feedback loop.
2. *Analyze, simulate and synthesize* noise and non-linearities in circuits.
3. *Analyze, simulate and synthesize* circuits which minimize device mismatch, particularly with mirrored circuits and devices in a differential circuit path.
4. *Design, simulate and synthesize* switched-capacitor building blocks for filter and data converter applications.
5. *Design, simulate and synthesize* all-CMOS phased-locked loops, and clocking circuitry, both VCO- and ring-oscillator based.
6. *Explore* Topics related to advanced and emerging CMOS transistors and packing.
7. *Understand* and apply the specifications and limitations of commercially available integrated circuits and systems intended for mass manufacturing of commercially available mm-Wave, RF, analog, digital, and mixed-signal circuits and systems.
8. *Understand* and apply the principles of modern IC design and the selection of semiconductor technologies, components, failure modes, reliability modes, mismatch analysis, and requirements in terms of size, cost and manufacturability.
9. *Design* Integrated Circuit (IC) building blocks such as bandgap circuits, low noise amplifiers, mixers, frequency synthesizers, and power amplifiers. These blocks will be designed to meet industry defined standards including performance over process voltage and temperature.
10. *Design* physical layouts to represent transistor level circuits. These layout designs will consider performance, manufacturability, cost and testability.
11. *Design* all circuits and layouts using industry accepted Computer Aided Design (CAD) tools such as Cadence, Altium and PSpice.

Additional Learning Objectives for EE 5xx, 5xx: At the end of this course, graduate students will be able to:

1. *Design and Plan* chip architecture as well as the system/application that the chip will be used for when applied to a specific application.
2. *Model* the entire chip architecture using Verilog-A or the equivalent system model tools.
3. *Lead* circuit design teams to bridge the gap between system definition and circuit topology implementation.

Textbook: B. Razavi, *Design of Analog CMOS Integrated Circuit*, 2nd edition, McGraw-Hill

Reference Textbooks:

1. P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 6th Ed., John Wiley & Sons, 2024.
2. B. Razavi, *RF Microelectronics*, 1st Ed., Prentice Hall, 1998.
3. M. E. Van Valkenburg, *Analog Filter Design*, Oxford University Press, 1982.
4. D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.

Topics:

1. Noise analysis (1 week)
2. Distortion analysis (1 week)
3. Switched-Capacitor design techniques (2 weeks)
4. Chip Tapeout Teaming Forming and Project Updates (2 weeks)
5. Analog Layout Techniques (2 weeks)
6. Advanced CMOS transistors and chip packaging issues (1 week)
7. EE 436 ends with a chip design progress report. (1 week)
8. Introduction to Systems on a Chip (SoCs) and applications (2 weeks)
9. Defining capstone projects using industry accepted figures of merit for the integrated electronics (e.g. noise figure, bandwidth, linearity/distortion, I/O interfaces) – (1 week)
10. Use of industry accepted analog and mixed-signal CAD tools – (1 week)
11. Introduction to good analog integrated circuit layout practices – (1 week)
12. Top-level planning and verification techniques – (2 weeks)
13. Exploration of analog and mixed-signal sub-systems such as clocking/phased-locked loops, switched-capacitor stages, data converters, to name a few. Topics are course dependent – (2 weeks)
14. Final project reviews and presentations – (1 weeks)

Course Structure: During the first quarter of the two-quarter sequence, the class meets twice a week, for a 110-minute lecture. Additionally, the class offers a 50-minute TA- or professor-led discussion session to emphasize course fundamentals and present examples. There are approximately three homework assignments that include small

SPICE/Spectre(RF) simulation tasks. Students will be assigned to teams of 3-4 students to develop project designs. Several project design reviews will be held throughout the first quarter.

In the second quarter, the class meets four times a week, for 50 minutes each. Each session will consist of lecture-style presentations and discussion of selected topics. The laboratory supports the completion of a quarter-long capstonec design project. The lab assignments are to be completed either in the Linux educational server room, in the ECE building, or work related to all projects can be done by remote access with a student's personal computer. Laboratory time is open for the student groups to use as needed. The capstone design project in EE 437 builds on prior work initiated by the teams designated in EE 436.

Laboratory Structure: The lab will consist of one large system-on-a-chip (SoC) project, that will include:

1. Initial system design and definition, to include specifications for circuit blocks.
2. Circuit design, simulation and verification.
3. Physical layout of circuit schematic.

Computer Resources: SpectreRF or HSPICE or PSPICE or Multisim may be used for circuit simulation; Mathcad or MATLAB or Mathematica may be used for general purpose mathematical analysis; Cadence schematic capture and layout; LabVIEW may be used for computer-controlled data acquisition and instrument control. Spectre, SpectreRF, Harmonic Balance, HSPICE, PSPICE, MATLAB, Multisim, and Ultiboard are available in all of the general-purpose computing laboratories in the ECE Department. LabVIEW is available in ECE 137 laboratory, integrated with hardware for data acquisition and instrument control.

Laboratory Resources: The main computer laboratory in the Electrical and Computer Engineering building will support this class with Linux-based computers that are networked to central servers at the University of Washington. All CAD software necessary to complete this design project will be found in the Cadence design environment. This will include the circuit, layout, and layout verification tools as well as the process design kit (PDK) which defines a semiconductor process to be selected by the student, based on cost, power and speed parameters.

Grading:

The grading for the undergraduates and graduate students in the combined two quarter class breaks down as follows:

- Homework – 5%
    - Grad students complete additional or more advanced problems (e.g., device-level modeling, advanced verification, layout optimization).
- Mini-project – 10%
    - Grad students must choose a more complex subsystem (e.g., a PLL instead of an op-amp, or an RF front-end instead of a simple ADC).
    - Grad students will be required to produce a short technical report including performance comparison to state-of-the-art.

- Midterm – 5%
    - Same exam, but with additional graduate-only questions worth up to 20–30% of the exam.
- Final Taped-Out Chip – 80%
    - Grad students must:
        - Implement additional blocks or increased system complexity
        - Provide more extensive verification (Monte Carlo, corner analysis, EM extraction, or behavioral/SystemVerilog modeling)
        - Produce a more formal design report (IEEE-style paper)

ABET Student Outcome Coverage:

This course addresses the following outcomes:

H = high relevance, M = medium relevance, L = low relevance to course.

(1) *An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.* **(H)** The vast majority of the lectures, homework and projects deal with the application of circuit theory and control theory to specific linear integrated circuit operation. Large- and small-signal semiconductor device characteristics are included in the formulations. Linear circuit analysis formulations are commonplace throughout the course. The homework and examinations involve solving engineering problems identified by the assignments and exemplified by class discussion. The design projects challenge the students to identify the issues and formulate their individual solutions. The projects are conducted in teams of two. Since both MOS and BJT technologies offer two major device options, each team member chooses one of the two options. The team submits a written report describing the individual designs and comparing the two alternative implementations.

(2) *An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.* **(M)** The course covers analysis and with emphasis on synthesis of linear integrated circuits, with associated homework and examination problems. To incorporate realistic constraints, a module on integrated circuit process variations and yield is taught.

(3) *An ability to communicate effectively with a range of audiences* **(H)** Design project reports are required to be styled and formatted like a product specification sheet. Emphasis is placed upon clear descriptions of circuit operation, illustrative system-level block diagrams, industry acceptable schematic diagrams, an estimate of die (chip) cost and formulation of cost estimates in a full high-volume production environment. The course ends with a poster presentation during the Electrical and Computer Engineering (ECE) capstone fair in addition to a 20 minute class presentation.

(4) *An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives* **(M)** The project design problems are addressed by teams of 3-4 students who must organize and divide up the work amongst themselves. Common partitions of work among students in a group include one student working on system definition, another working on circuit simulation, and another focusing on physical layout.

(5) *An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions*. **(M)** Students use SPICE to simulate homework problems and to support design projects. The course involves direct experience with the design of semiconductor integrated circuits and experimentation with simulation software. Students must devise their own projects and define their own simulations to verify their designs and make engineering judgments based on those outcomes of those simulations, then redesign the system/components as necessary.

(6) *An ability to acquire and apply new knowledge as needed, using appropriate learning strategies* **(M)** The course focuses on modern electronic circuit design which involves researching, selecting and designing components using prior state-of-the-art designs as a starting point. Students are responsible for learning this on their own.

Religious Accommodations Policy

Washington state law requires that UW develop a policy for accommodation of student absences or significant hardship due to reasons of faith or conscience, or for organized religious activities. The UW's policy, including more information about how to request an accommodation, is available at Religious Accommodations Policy. Accommodations must be requested within the first two weeks of this course using the Religious Accommodations Request form.

Accommodations and Access

If you have already established accommodations with Disability Resources for Students (DRS), please communicate your approved accommodations to me at your earliest convenience so we can discuss your needs in this course. If you have not yet established services through DRS, but have a temporary health condition or permanent disability that requires accommodations (conditions include but not limited to; mental health, attention-related, learning, vision, hearing, physical or health impacts), you are welcome to contact DRS at 206-543-8924 or uwdrs@uw.edu or disability.uw.edu. DRS offers resources and coordinates reasonable accommodations for students with disabilities and/or temporary health conditions. Reasonable accommodations are established through an interactive process between the student, instructor, and DRS. It is the policy and practice of the University of Washington to create inclusive and accessible learning environments consistent with federal and state law.

Academic Integrity

Engineering is a profession demanding a high level of personal honesty, integrity and responsibility. Therefore, it is essential that engineering students, in fulfillment of their academic requirements and in preparation to enter the engineering profession, adhere to the College of Engineering Statement of Principles. Any student in this course suspected of academic misconduct (e.g., cheating, plagiarism, or falsification) will be reported to the College of Engineering Dean's Office and the University's Office of Community Standards and Student Conduct to initiate the student conduct process.

Title IX

UW, through numerous policies, prohibits sex- and gender-based violence and harassment, and we expect students, faculty, and staff to act professionally and respectfully in all work, learning, and research environments. For support, resources, and reporting options related to sex- and gender-based violence or harassment, visit UW Title IX's webpage (https://www.washington.edu/titleix/), specifically the Know Your Rights & Resources guide (https://www.washington.edu/titleix/files/2020/08/KYRR-guide-8-10-2020-LINKED.pdf).

If you choose to disclose information to me about sex- or gender-based violence or harassment, I will connect you (or the person who experienced the conduct) with resources and individuals who can best provide support and options. You can also access those resources directly:

- Confidential: Confidential advocates (https://www.washington.edu/sexualassault/support/advocacy/) will not share information with others unless given express permission by the person who has experienced the harm or when required by law.
- Private and/or anonymous: SafeCampus (https://www.washington.edu/safecampus/) provides consultation and support and can connect you with additional resources if you want them. You can contact SafeCampus anonymously or share limited information when you call

Please note that some senior leaders and other specified employees have been identified as "Officials Required to Report." (https://www.washington.edu/titleix/title-ix-officials-required-to-report/) If an Official Required to Report learns of possible sex- or gender-based violence or harassment, they are required to call SafeCampus and report all the details they have in order to ensure that the person who experienced harm is offered support and reporting options (https://www.washington.edu/titleix/resources/)."