# ECE  IS & VLSI Curriculum Review
# Spring 2024 – Winter 2025

Chris Rudell

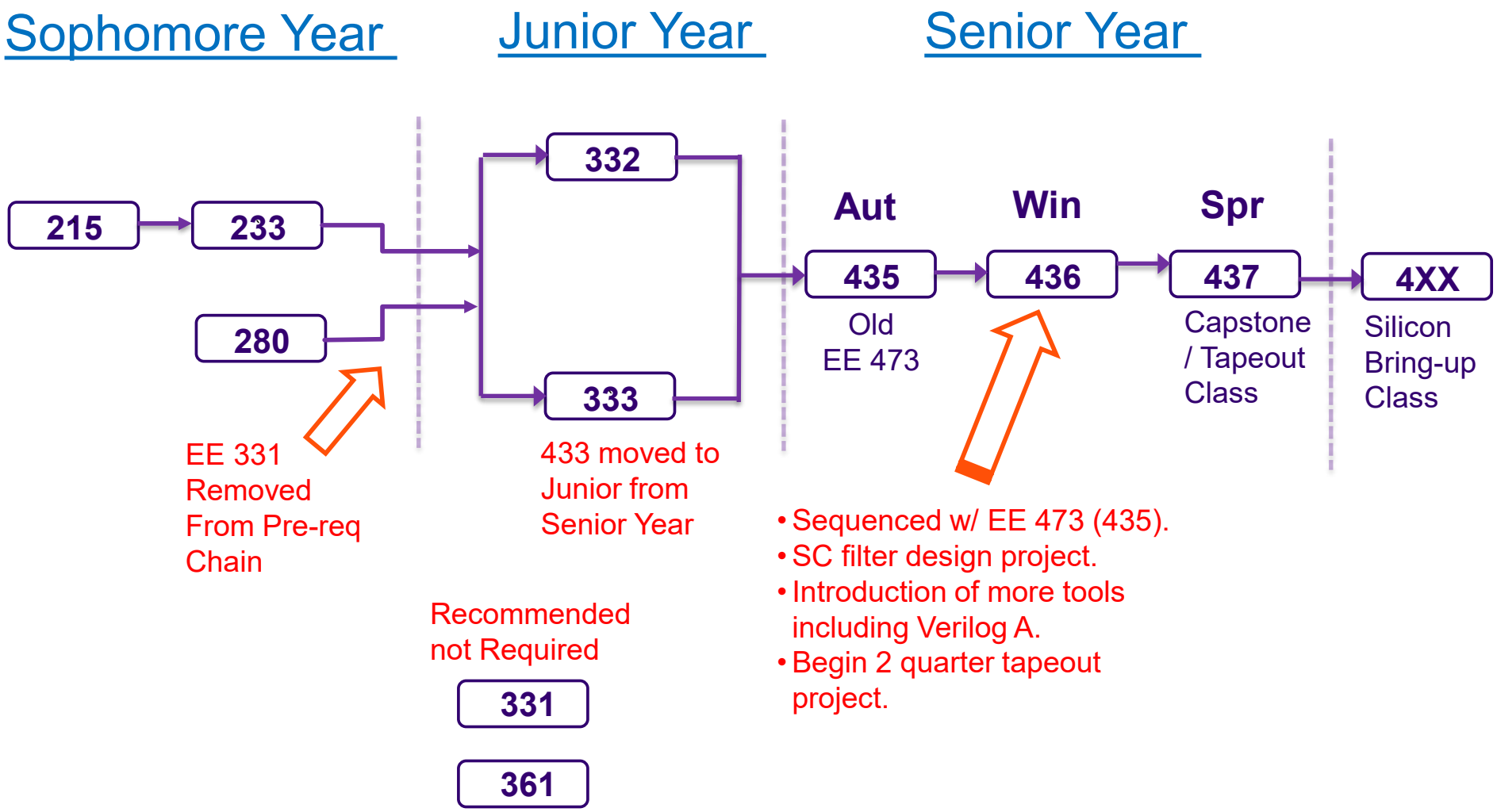
ELECTRICAL & COMPUTER ENGINEERING

# 2026 Faculty in VLSI

- Full-time ECE/VLSI Appointments:
  - Richard Shi - IC, Test, CAD
  - Michael Taylor - Digital VLSI, Computer Architecture
  - Sajjad Moazeni - IC design, Analog, Integrated Nano-Photonics
  - Chris Rudell - IC, Analog, RF, & mm-Wave
  - Hossein Naghavi - Analog, Analog IC Design, mm-Wave, subTHz, E&M
  - Tai Chen - Analog & Digital, General
  - Ang Li - Digital Circuits, Computer Architecture
  - Rania Hussein - General/Embedded

- Partial ECE/VLSI Appointments:
  - Matt Reynolds
  - Shwetak Petal
  - Josh Smith
  - Georg Seelig

# New Integrated Systems Pathway



# Enrollment in IS and VLSI : 2024 – 2026

| | | Aut24 | Win25 | Spr25 | Aut25 | Win26 | Spr26 |
|---|---|---|---|---|---|---|---|
| **332** | **Devices & Circuits II** | 14 | | 28 | 46 | | 35 |
| **333 (433)** | **Analog Embedded Systems** | | 26 (old 433) | | | | 38 |
| **437/400/538** | **Integrated Systems Capstone** | | | 5/5/9 | | | 18/0/8 |
| **473/538** | **Linear Integrated Circuits** | 5/16 | 19/8 | | 21/7 | | |
| **476** | **Introduction to Very Large-Scale Integrated Design** | 71 | | | 80/61 | | |
| **477/525** | **VLSI II (w/ CSE in Win 23)** | | 28/23 (CSE 4) | | | 61 | |
| **478/526** | **Capstone Integrated Digital Design Projects** | 26 | | | | | |

- Significant enrollment increases in EE 332 and EE 473 (now 435)
- EE 476-477-478 Enrollment continues to increase.
- EE 333 (was 433) has become a popular class since Hossein took it over.

# End of Course Evaluations

| Course | Qtr. | Intructor | Particiapted | Adj. Combined | CEI | Hours/Cr |
|---|---|---|---|---|---|---|
| **332** | Autumn 2025 | Moazeni | 11/12 | 4.1 | 5.2 | 2.1 |
| **332** | Spring 2025* | Naghavi | 27/45 | 4.4 | 5.1 | 2.4 |
| **333** | Winter 2025 | No report available | | | | |
| **436/598** | Winter 2026 | Rudell | 21/24 | 3.2 | 6.0 | 3.2 |
| **437/538** | Spring 2025 | Rudell | 15/16 | 3.5 | 6.9 | 4.5 |
| **433 (now 333)** | Winter 2024 | No report available | | | | |
| **473/538** | Autumn 2025 | Rudell | 27/28 | 3.5 | 5.6 | 2.2 |
| **476** | Autumn 2025 | Li | 63/72 | 3.8 | 6.1 | 3.8 |
| **477/525** | Winter 2024 | Li | 48/61 | 3.9 | 5.1 | 2.3 |
| **478/526** | Spring 2025 | Li | 17/26 | 4.3 | 5.5 | 1.9 |

- Reviews continue to improve in Ang's classes (476/477/478)
- First time Hossein taught EE 332, his review scores were very high.
- Review scores struggle for Chris, as course (473/436/437) have been made significantly harder with new tapeout program.

# End-of-Course Reports

| Course | Title | Instructor | Quarter | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 332 | Devices & Circuits II | Naghavi | Spr25 | | | | | | | | NA: not assigned |
| 332 | Devices & Circuits II | Moazeni | Aut25 | | | | | | | | NA: not assigned |
| 436/598 | Integrated Systems Capstone I | Rudell | Win26 | 2/0/0/2 | 2/0/0/2 | 2/0/0/2 | | | | | Submitted |
| 437/538 | Integrated Systems Capston II | Rudell | Spr25 | | 0/0/0/3 | 0/0/0/3 | | 0/0/0/3 | 0/0/3/0 | 0/0/0/3 | |
| 473/538 | Linear Integrated Circuits | Rudell | Aut25 | | | | | | | | NC: not completed |
| 476 | Introduction to Very Large-Scale Integrated Design | Ang Li | Aut25 | 1/3/6/2 | | 1/5/4/2 | | 1/5/4/2 | | | |
| 476 | Introduction to Very Large-Scale Integrated Design | Richard Shi | Win26 | | | | | | | | NC: not completed |
| 477/525 | VLSI II | Ang Li | Win26 | | | | | | | | NA: not assigned |
| 478/526 | Capstone Integrated Digital Design Projects | Ang Li | Spr25 | 0/0/3/3 | 0/0/4/2 | | | 0/0/4/2 | 0/0/3/3 | 0/0/4/2 | |

# Comments

- **TAs in the IS and VLSI area:** Lecturers live and die by good or bad TAs. Generally, we need TAs that are very skilled in both circuits, architecture, linux and CAD Tools, mainly Cadence. With the TAs class in IS and VLSI would cease to exist.
- **Demand on TAs time:** The demand on TAs time far exceeds what a normal TA may encounter. This is a combination of students taking the classes who are not well prepared, and the nature of IC design (digital and analog).
- **Labs: Labs in IS and VLSI:** New IS/VLSI Linux on the 3rd now has excellent compute power and is very nice space. However, if both tapeout classes continue the same growth patterns, we are definitely going to need more space.

# Final Thoughts.

- IS Track continues to see students with very poor fundaments that simply cannot be expected to tapeout an analog chip – some students cannot recognize Ohm's Law.
- New Faculty are doing great: - Hossein and Ang are quickly becoming the strongest lecturers in the department.
- IS Curriculum revamp is basically done. Can now see new course numbers (grad and undergrad) online. .
- Tapeout classes are popular with students (although very, very hard) and industry. IS had final chip design review yesterday with 10-ish engineers from Boeing, Amazon and Apple in attendance.