
EEP 535: DIGITAL SYSTEMS DESIGN WITH FPGAS (4cr)

Summary:

Recent trends have shown a clear need for technologies that offer rapid prototyping, programmability, and re-use capabilities. When developing embedded systems with the above capabilities, various components are used, including computer processors/microcontrollers, Field Programmable Gate Arrays (FPGAs), memory, and input/output peripheral devices, to name a few. FPGAs tend to be the go-to platforms to increase the processing speed for hardware acceleration in applications such as Genomic research, financial analysis, and video processing. This course focuses on using FPGAs to design digital systems. By the end of this course, you will be able to design digital systems by understanding FPGA architectures and their design flow.

Prerequisite:

- Familiarity with Java or C++: Including but not limited to: data abstraction and encapsulation, including stacks, queues, linked lists, binary trees, recursion, and use of predefined collection classes.
- Basic Knowledge of electrical circuits.

- **Instructor:**

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- **Sep Makhsous**, sosper30@uw.edu
 - **Office hours:** By Appointment

- **TA:**

- **Alperen Cuci**, cuci@uw.edu
 - **Office Hours:** see Lab Hours

Main Communication Platform: Slack Link (This is mandatory for all students): [CLICK HERE](#)

Class Meetings Information:

- **Lecture:**

- TTh 4:30p-6:20p, ECE 269
- **Lecture Format:**
 - The first hour, the lecture
 - The second hour, In-Class Team Exercises (ICTE) (more info below).
- **Labs:**
 - Lab Hours

Grading policy:

- Homework: 20%
 - ICTEs: 10%
 - Labs: 50%
 - Midterm: 20%
 - Bonus: 5%
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Class format:

The class will be held in person. It is important that you attend the class meetings to increase your learning experience, especially during In-Class Team Exercises (ICTE) (more info below). We will provide, prefilled slides, recorded lectures, and filled-out notes for you to review asynchronously. We will also provide a zoom option for those who can not make it in person; however, this is not a hybrid course, hence, the engagement through zoom will be limited. If you are joining the class remotely, you will need to make sure to collaborate with your team during ICTEs to receive full credit.

FAQ

Q: *What should I do if I can't come in person to a class meeting.?*

A: Connect to the class Zoom -- you will be able to listen to the lecture. Coordinate with your team and join them remotely during ICTEs.

Q: *Are office hours remote or in person?*

A: Unless otherwise announced, all office hours offered by the TA and the Instructor will be held remotely via Zoom.

Q: *How do I access class recordings?*

A: Canvas, under the Zoom tab

Overview

Learning Outcomes [LO] -- by the end of this course, you will be familiar with:

1. Combinational Logic Design
 2. Sequential Logic Design
 3. Algorithmic State Machine (ASM)
 4. Finite State Machines
 5. Clock Domain Crossing and Meta-stability
 6. EDA tools and System Verilog
 7. FPGA Architecture
 8. FPGA Design Process
 9. FPGA Logic Implementation and Features
 10. FPGA Timing Analysis
 11. FPGA Constraints
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Course materials

We will provide lecture notes, homework assignments, and other materials using Canvas Home Page,

Here is a summary of all the course material:

- **Prefilled slides:** will be posted 12 hours prior to the lecture
- **ICTEs:** will be posted during the lecture and will be due by the end of class time
- **HW:** will be posted at least 1 week prior to the deadline and will be due on Friday at midnight
- **Filled out Lectures and Recordings:** will be posted 12 hours after the lecture
- **Labs:** will be posted at least 2 weeks prior and will be due on Friday at midnight.

- Keep in mind you have 1 week to complete your demos after submitting the reports.

Textbook references

There is no required textbook for this course, i.e. **you do not need to purchase a textbook.** Lecture notes will be provided on canvas

I will draw material from several references about digital systems and circuits:

Hauck, Scott, and Andre DeHon. Reconfigurable computing: the theory and practice of FPGA-based computation. Elsevier, 2010.

Harris, Sarah L., and David Harris. Digital design and computer architecture. Morgan Kaufmann, 2015.

Vahid, Frank. Digital design with RTL design, VHDL, and Verilog. John Wiley & Sons, 2010.

Homework

See the Canvas home page for homework assignments and deadlines.

Workload: **there will be a(n) (almost) weekly homework assignment** posted and submitted in electronic form as a .pdf on Canvas There will be approximately six (6) homework assignments, and they will account for 20% of the grade. Homeworks are done in teams.

In-Class Team Exercises (ICTE)

Will be published on Canvas for the second part of the lecture. ICTEs are in-class assignments done in groups and submitted by the end of class.

Workload: **there will be approximately one ICTE per week.**

Labs

You will work on four (4) labs during this course.

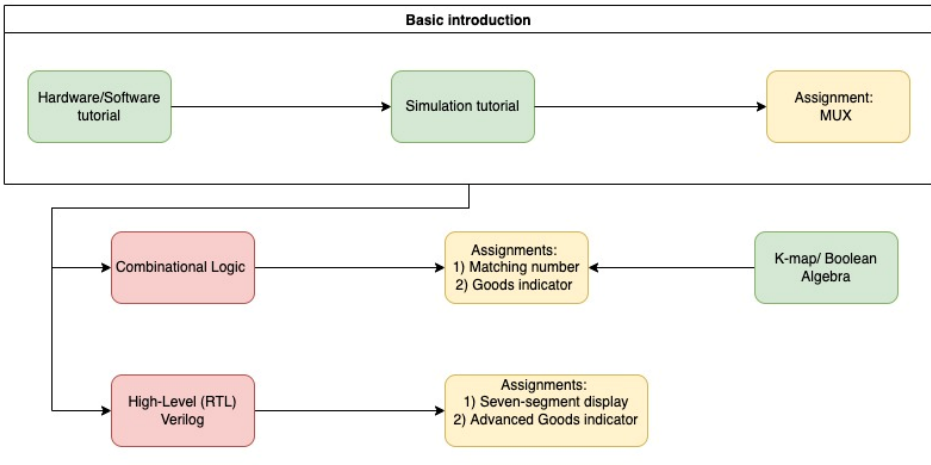
Labs are done in teams, you will need to start on the labs as soon as possible, there will be no extensions on the labs, and late submissions will result in an automatic 0.

Labs are an integral portion of the class learning. Failure to make a good-faith effort at the labs is grounds for failing the class.

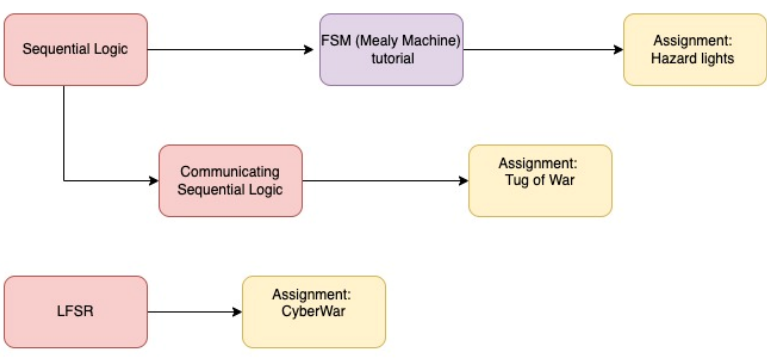
Lab kit pick up: Lab kits can be picked up from the TAs. Please make sure to test your lab kits by going through the Quartus/Verilog tutorials in advance of working on Lab 1.

Below you can see the diagram which lays out the learning objectives for each lab. Keep in mind, labs are an important part of your class; you need to start early and make sure everyone in the team contributes equally.

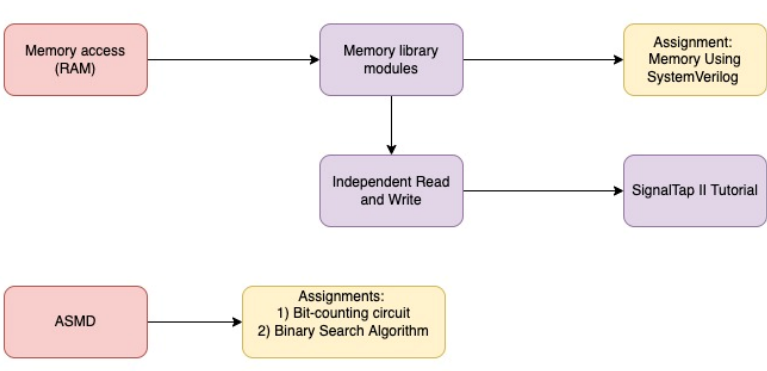
Lab1



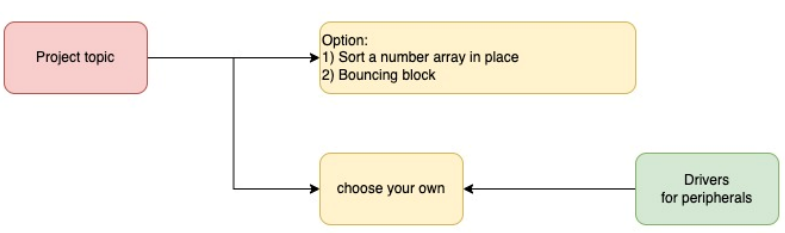
Lab2



Lab3



Final Project



Collaboration guidelines

Done in teams: Homework assignments and ICTEs - Groups of 2

Done Individually: Labs and quizzes, Midterm

In addition, you are welcome (and encouraged) to:

- work together, synchronously and asynchronously, in study groups;
- use analytical and numerical computational tools -- specify the tool(s) in source code and/or text;
- reuse example source code and other materials provided in this course;
- consult textbooks, websites, and other publicly-available materials -- include a full citation(s) with the URL and/or [DOI \(Links to an external site.\)](#).

Submission guidelines

You will submit your homework write-up by uploading a .pdf on the Canvas Assignment. **We will only grade legible .pdf files -- we will not grade content in any other file format (.doc, .zip, .ipynb, .m, ...).**

If you write your solutions by hand, you must create a legible scan; if you have any doubts about the fidelity of your scans, send a sample to the instruction team in advance of the homework deadline.

<http://www.howtogeek.com/209951/the-best-ways-to-scan-a-document-using-your-phone-or-tablet/> (Links to an external site.)

Midterm

There will be one take-home midterm.

The midterm will be worth 20% of the grade.

You are welcome (and encouraged) to:

- Consult textbooks, websites, and other publicly-available materials -- include a full citation(s) with the URL and/or DOI (Links to an external site.).
- By submitting your quiz solution on Canvas, you are affirming your understanding of and adherence to these restrictions.

- Any signs of cheating will result in an automatic zero for all involved students.

I accept queries for regrades on specific exam problems for 1 week via written requests.

Due dates and extensions

Due date: homework assignments are **due by 11.59pm on Saturday**. You will receive 5% bonus if you submit on time

- Late submissions are accepted by **11:59p on Sunday**. no bonus points
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Grade

As described above, the final grade will be determined from:

- Homework: 20%
 - ICTEs: 10%
 - Labs: 50%
 - Midterm: 20%
 - Bonus: 5%
 - **Total: 105%**
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Canvas and Slack

We will use Canvas (i.e. this site) extensively for course materials and **Slack for all communications**.

The instruction team will provide homework, example code, etc., through Canvas; you will submit homework electronically through Canvas as described above.

If you have a question -- about a concept, HW problem, etc. -- it's likely someone else in the class does as well. **Please use our Slack channel to post questions (rather than emailing or messaging the instruction team directly) so that (a) others get to propose answers and (b) others get to see the definitive answer (if any)**. If you send questions via email to the instruction team, we will direct you to ask it on Slack so others can benefit from our answers.

If you are unfamiliar with Canvas, here are some links to help you get started:

<https://www.tacoma.uw.edu/canvas/getting-started>Links to an external site.

<https://www.tacoma.uw.edu/canvas/how-do-i>Links to an external site.

<https://community.canvaslms.com/community/answers/guides/> (Links to an external site.)

Diversity, Equity, and Inclusion

I consider this classroom to be a place where you will be treated with respect, and I welcome individuals of all ages, backgrounds, beliefs, ethnicities, genders, gender identities, gender expressions, national origins, religious affiliations, sexual orientations, abilities – and other visible and non-visible differences. All members of this class, including instructors, are expected to contribute to a respectful, welcoming, and inclusive environment for every other member of the class.

Disability and access accommodations

Your experience in this class is important to me. If you have already established accommodations with Disability Resources for Students (DRS), please communicate your approved accommodations to me at your earliest convenience so we can discuss your needs in this course.

If you have not yet established services through DRS, but have a temporary health condition or permanent disability that requires accommodations (conditions include but are not limited to; mental health, attention-related, learning, vision, hearing, physical or health impacts), you are welcome to contact DRS at 206-543-8924 or uwdrs@uw.edu or disability.uw.edu ([Links to an external site.](#)). DRS offers resources and coordinates reasonable accommodations for students with disabilities and/or temporary health conditions. Reasonable accommodations are established through an interactive process between you, your instructor(s) and DRS. It is the policy and practice of the University of Washington to create inclusive and accessible learning environments consistent with federal and state law.

Religious accommodations

Effective July 28, 2019, [Washington State Senate Bill 5166](#) ([Links to an external site.](#)) required that UW develop a policy for the accommodation of student absences or significant hardship due to reasons of faith or conscience, or for organized religious activities. I am proud that my

UW ECE colleague [Rania Hussein](#) [Links to an external site.](#) contributed to drafting and promoting this legislation.

The UW's policy, including more information about how to request an accommodation, is available at Faculty [Syllabus Guidelines and Resources](#) [\(Links to an external site.\)](#).

Accommodations must be requested within the first two weeks of this course using the Religious Accommodations Request form available

at: <https://registrar.washington.edu/students/religious-accommodations-request/> [\(Links to an external site.\)](#)

Safety

Call SafeCampus at 206-685-7233 anytime – no matter where you work or study – to anonymously discuss safety and well-being concerns for yourself or others. SafeCampus's team of caring professionals will provide individualized support while discussing short- and long-term solutions and connecting you with additional resources when requested.

Academic misconduct

Engineering is a profession demanding a high level of personal honesty, integrity, and responsibility. Therefore, it is essential that engineering students, in fulfillment of their academic requirements and in preparation to enter the engineering profession, shall adhere to the University of Washington's [Student Code of Conduct](#) [\(Links to an external site.\)](#).

Any student in this course suspected of academic misconduct (e.g., cheating, plagiarism, or falsification) will be reported to the College of Engineering Dean's Office and the University's Office of Community Standards and Student conduct. (See [CoE website](#) [\(Links to an external site.\)](#) for a more detailed explanation of the academic misconduct adjudication process). Any student found to have committed academic misconduct will receive a 0-grade on impacted academic work (e.g., assignments, projects, or exams).